IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PRIORITY Application Serial No. 09/507,193
PRIORITY Filing Date .....February 18, 2000
Inventor.....Mark Fischer et al.
Assignee .....Micron Technology, Inc.
PRIORITY Group Art Unit 1765
PRIORITY Examiner .....D. Deo
Attorney's Docket No. MI22-1777
Title: Semiconductor Processing Methods of Forming a Conductive Projection and Methods of Increasing Alignment Tolerances

Preliminary Amendment to Accompany the filing of a Continuation Application Under 37 C.F.R. 1.53(b)

To: Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

From: Bernard Berman (Tel. 509-624-4276; Fax 509-838-3424)
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Sir:

This is a preliminary amendment accompanying a Request for Continuation Application for the above-entitled patent application. Prior to examining the application, please enter the amendments and consider the remarks contained herein.

AMENDMENTS

In the Specification

Please replace the indicated paragraphs with the following clean version of each paragraph, in accordance with 37 C.F.R. § 1.121(c)(1)(i). A marked up version showing the amendment(s) is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. § 1.121(c)(1)(ii).

On page 1, after the title and prior to the "Technical Field", insert:

-- **RELATED PATENT DATA**

This patent resulted from a continuation application of U.S. Patent Application Serial No. 09/507,173 filed on February 18, 2000.--

In the Claims

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 C.F.R. § 1.121(c)(1)(i). Cancel all previous versions of any pending claim.

A marked up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. § 1.121(c)(1)(ii). Any claim not accompanied by a marked up version has not been changed relative to the immediate prior version, except that marked up versions are not being supplied for any added claim or canceled claim.

CLAIMS

Cancel Claims 1-11.

12. (Amended) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface; and

unevenly removing material from the first uppermost surface of the conductive plug to define an uneven second uppermost surface at least a portion of which is disposed elevationally higher than the conductive lines and to reduce a width of the conductive plug from what it was prior to said unevenly removing.

13. The method of claim 12, wherein the unevenly removing material of the conductive plug comprises facet etching the conductive plug.

Cancel Claims 14-15.

16. The method of claim 12, wherein the forming of the conductive plug comprises forming the uneven uppermost surface of the plug to have a central region and a corner region joined therewith, and the unevenly removing material comprises removing more material from the corner region than from the central region of the first uppermost surface.

Cancel Claims 17-20.

21. (Amended) A method of increasing alignment tolerances between bit line contact material and storage capacitors in a DRAM comprising beveling at least one corner of a conductive plug formed over a diffusion region with which a bit line is to electrically communicate effectively to reduce a width of the conductive plug, the beveling changing a first generally even uppermost surface to a second generally uneven uppermost surface.

22. (Amended) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface having a generally uniform surface and having a width; and

etching material of the conductive plug to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines and to reduce the width of the conductive plug.

23. The method of claim 22, wherein the etching of the material of the conductive plug comprises facet etching the conductive plug.

Cancel Claims 24-46.

47. The method of claim 21 comprising beveling at least two corners of the conductive plug.

48. (Amended) A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching; and

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections.

49. (Amended) The method of claim 48 comprising etching both of the conductive contact projections to reduce their widths.

50. The method of claim 48 wherein the etching comprises at least etching at least one outermost corner of the at least one conductive contact projection.

52. The method of claim 12 wherein the unevenly removing comprises removing material of the conductive plug from an entirety of the uppermost surface.

53. The method of claim 12 wherein the uppermost surface is substantially planar immediately prior to the unevenly removing.

54. (Amended) The method of claim 21 wherein the beveling is effective to reduce a height of the conductive plug over the diffusion region.

55. The method of claim 22 wherein the etching etches material of the conductive plug from an entirety of the uppermost surface.

56. The method of claim 22 wherein the uppermost surface is substantially planar immediately prior to the unevenly removing.

Cancel Claims 57-60.

61. The method of claim 48 wherein the one projection has an uppermost surface and the etching of the one projection etches material of the one projection from an entirety of the uppermost surface.

62. The method of claim 48 wherein at least the one projection has an uppermost surface which is substantially planar immediately prior to the etching of the one projection.

63. The method of claim 48 wherein the conductive projections have outermost surfaces which are entirely outwardly exposed during the etching of the at least one projection.

Cancel Claims 64-67.

Add Claim 68.

--68. A method of forming DRAM circuitry comprising:

forming a pair of spaced-apart, insulated conductive lines over a substrate, the conductive lines defining a node location therebetween;

forming insulative material over the node location and between the conductive lines;

forming an opening through the insulative material and between the lines to proximate the node location;

forming conductive material within the opening over the node location, the conductive material comprising an outer portion received elevationally outward of the insulated conductive lines, the conductive material having side surfaces which project away from the node location and terminate proximate an upper surface, the side surfaces and upper surface defining at least one corner region, the side surfaces defining a maximum width of the outer portion of the conductive material within the opening; and

beveling the at least one corner region effective to reduce the maximum width of the outer portion of the conductive material above the conductive lines and etching at least some of the conductive material away from an entirety of the upper surface.

REMARKS

Claims 12-13, 16, 21-23, 47-50, 52-56, 61-63 and 68 are presented herein for examination. Claims 12-13, 16, 21-23, 47-50, 52-56 are amended from the priority application, as indicated, to conform with the agreement reached with the priority Examiner, as described below. Claim 68 is a new claim not subject to the aforementioned agreement.

During a telephonic interview conducted on July 16, 2001, the undersigned and priority Examiner Deo reached an agreement regarding a rejection under §112, second paragraph, of claims in the priority application. At issue was the use of the word "maximum" referring to either width or height. Examiner Deo's position was that what Applicant believed was a maximum dimension, another person might consider a minimum dimension unless some value for maximum was claimed. The undersigned explained that in the context of the priority application the terms "maximum width" or "maximum height" refer to a largest width or height and not to a specific value for either dimension. Applicant's usage being consistent with the dictionary definition provided in *Merriam-Webster's Collegiate Dictionary,* Tenth Edition, page 718, which is "the greatest quantity or value attainable." Not withstanding the definition provided, resolution of this impasse was achieved by deleting the word "maximum" from the claims, thus such amended claims were allowed in the priority application. As some of the claims presented herein for examination are canceled claims from the priority application that were also subject to the above-referenced rejection, such claims are similarly amended to delete

the word "maximum." Applicant respectfully asserts that the scope of such claims is unchanged by the amendment and any limitation of that scope resulting from such amendment is inappropriate.

Rejections under 35 U.S.C. §103(a):

In the Final Office Action of the priority application, Claims 12, 13, 16, 21-23 and 47 stood rejected under 35 U.S.C. §103(a) as being unpatentable over Crotti (US 4,957,881). In addition, Claims 48-50 stood rejected under 35 U.S.C. §103(a) as being unpatentable over Crotti and further in view of Fazan et al. (US 5,597,756, hereinafter "Fazan"). Such claims, as well as Claims 52-53 depending from Claim 12, Claim 54 depending from Claim 21, Claims 55-56 depending from Claim 22 and new Claim 56, are presented herein. Applicant respectfully requests that the examination of such claims be conducted in view of the remarks presented below.

Crotti

Applicant's Claims 12, 21 and 22 each recite, respectively and in pertinent part, "the conductive plug having a first uppermost surface; and unevenly removing material from the first uppermost surface of the conductive plug to define an uneven second uppermost surface," "the beveling changing a first generally even uppermost surface to a second generally uneven uppermost surface" and "the conductive plug having a first uppermost surface having a generally uniform surface and having a width; and etching material of the conductive plug to define a second

uppermost surface which is generally non-planar." Thus each of these independent claims, from which Claims 13, 16, 22, 23 and 47 respectfully depend, includes an aspect of changing a first uppermost surface to a second uppermost surface.

In contrast, Crotti, as depicted in Figs. 4-8 defines forming a matrix metal layer 7 and etching such layer 7 using residues of planarization SOG material 8 that is defined along the bottom of valleys of the previously deposited layer 7. As Crotti describes, the etching is conducted for a time sufficient to form the structure shown in Fig. 6 (col. 3, lines 49-58). Thus the structure shown in Fig. 6 has the same uppermost surface as the original, unetched metal layer 7 shown in Fig. 4, SOG material 8 serving as an etch mask or protector for that uppermost surface. In Fig. 7, Crotti teaches forming a dielectric layer 9 overlying the structure of Fig. 6, and in Fig. 8, Crotti teaches the etching of layer 9, which also removes SOG material 8, to expose an uppermost surface of metal layer 7. Crotti never teaches or even suggests that a conductive plug is formed having a first uppermost surface which is modified in any manner to form a second uppermost surface as is essentially recited in each of Applicant's Claims 12, 21 and 22.

The priority Examiner responded to the above remarks by stating of Crotti that "Figures 3 and 6 would certainly shows two uppermost surface, the before and after (or claimed 1st and 2nd surfaces)" (second full paragraph on page 5 of the Final Office Action). However, looking at the referred to figures, it is seen that Fig. 3 is "a schematic plan view of a self-

aligned contact made in accordance with the [Crotti] invention" (col. 2, lines 12-13), while Fig. 6 is the third of six cross sectional figures that are used to depict the Crotti process (see, ibid., lines 14-15). Thus Applicant respectfully asserts that the priority Examiner's comparison of a plan view of the completed structure, to a cross sectional view of a partially formed structure, is an inappropriate comparison and cannot possibly show two uppermost surfaces, the before and after, as alleged. Furthermore, as Applicant previously stated and as is shown in Fig. 6, metal layer 7 is covered with SOG material 8 thus an uppermost surface of metal layer 7 is completely protected during the etching of other portions of such layer. Such protection is evidenced where Crotti describes that material 8 defines the "length" of the contact by a non-critical masking step (col. 3, lines 23-30), since to retain this defined length, shown in Fig. 3, the uppermost surface of layer 7 CANNOT be etched. Hence Crotti CANNOT and DOES NOT teach or even suggest "unevenly removing material from the first uppermost surface of the conductive plug to define an uneven second uppermost surface," "the beveling changing a first generally even uppermost surface to a second generally uneven uppermost surface" or "etching material of the conductive plug to define a second uppermost surface which is generally non-planar" as recited, respectfully, in Claims 12, 21 and 22.

M.P.E.P. §2403.03 states that "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580

(CCPA 1974)." Since it is shown that Crotti fails to teach or even suggest at least the above aspects of Applicant's invention recited in Claims 12, 21 and 22, a rejection of any of such claims, or any claim depending from such claims, based on Crotti, is incorrect.

Crotti in view of Fazan et al.

Applicant's Claim 48 recites, among other things, "the conductive contact projections having respective maximum widths and a generally even first uppermost surface; etching at least one of the conductive contact projections effective to reduce its maximum width, and form a generally uneven second uppermost surface."

As remarked above, Crotti DOES NOT teach or even suggest the forming of a first uppermost surface and etching that surface to form a second uppermost surface. Hence Crotti CANNOT teach or suggest the above recited aspect of Claim 48.

Turning to Fazan, the priority Examiner alleged that it would be obvious to one skilled in the art to modify Crotti in light of Fazan since Fazan teaches forming several conductive plugs, and the forming and etching of an insulating layer on the conductive plugs. Fazan does provide a teaching that shows multiple conductive plugs 18A and 18B, forming an insulating material stack 26 and etching stack 26 to form openings 32 that expose an uppermost surface of plugs 18A and 18B, However, Figs. 1-3 indicate that the uppermost surfaces of such plugs are unchanged during the processing. This lack of change is supported by Fazan at col. 3, line 15 - col. 4, line 13, cited by the priority Examiner, as there is no teaching

or suggestion that the etching process used to form openings 32 would affect plugs 18A or 18B in any manner. Therefore, Fazan also does not teach or even suggest forming a first uppermost surface and etching that surface to form a second uppermost surface as recited, essentially, by Claim 48.

Contrary to the priority Examiner's allegation, since neither Crotti nor Fazan teach or suggest individually at least this one aspect of Claim 48, it is inconceivable that a combination of Crotti with Fazan could provide such a teaching or suggestion. Thus in accordance with M.P.E.P §2403.03, as cited above, any rejection of Claim 48, or any claim that depends therefrom, must be incorrect if based on Crotti in view of Fazan.

In summary, Applicant having has provided remarks that are germane to each of Crotti and Fazan individually as well as in any combination. Such remarks show that Crotti taken alone or in view of Fazan DOES NOT provide any teaching or suggestion that can provide the basis of a rejection under §103(a). Hence, Applicant respectfully asserts that Claims 12-13, 16, 21-23, 47-50, 52-56, 61-63 and 68 are in condition for immediate allowance, which action is earnestly sought. If, however the Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic interview. The undersigned is available during normal business hours, Pacific Coast Time.

Respectfully submitted,

Dated: July 18, 2001 By: ______________________

Bernard Berman
Reg. No. 37,279

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Filing Date .....February 18, 2000
Inventor.....Mark Fischer et al.
Assignee .....Micron Technology, Inc.
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Examiner .....D. Deo
Attorney's Docket No. MI22-1777
Title: Semiconductor Processing Methods of Forming a Conductive Projection and Methods of Increasing Alignment Tolerances

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO DECEMBER 6, 2000 OFFICE ACTION

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Cancel Claims 1-11.

12. A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface; and

unevenly removing material from the first uppermost surface of the conductive plug to define an uneven second uppermost surface at least a portion of which is disposed elevationally higher than the conductive lines and to reduce a ~~maximum~~ width of the conductive plug from what it was prior to said unevenly removing.

Cancel Claims 14-15.

Cancel Claims 17-20.

21. A method of increasing alignment tolerances between bit line contact material and storage capacitors in a DRAM comprising beveling at least one corner of a conductive plug formed over a diffusion region with which a bit line is to electrically communicate effectively to reduce a ~~maximum~~ width of the conductive plug, the beveling changing a first generally even uppermost surface to a second generally uneven uppermost surface.

22. A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface having a generally uniform surface and having a ~~maximum~~ width; and

etching material of the conductive plug to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines and to reduce the ~~maximum~~ width of the conductive plug.

Cancel Claims 24-46.

48. A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective ~~maximum~~ widths and a generally even first uppermost surface;

etching at least one of the conductive contact projections effective to reduce its ~~maximum~~ width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching; and

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections.

49. The method of claim 48 comprising etching both of the conductive contact projections to reduce their ~~maximum~~ widths.

54. The method of claim 21 wherein the beveling is effective to reduce a ~~maximum~~ height of the conductive plug over the diffusion region.

Cancel Claims 57-67.

Add Claim 68.